

Docket No.: M4065.0216/P216-B  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re Patent Application of:  
Kie Y. Ahn et al.

Application No.: Not Yet Assigned

Filed: Concurrently Herewith

Art Unit: N/A

For: SYSTEM-ON-A-CHIP WITH MULTI-  
LAYERED METALLIZED THROUGH-  
HOLE INTERCONNECTION

Examiner: Not Yet Assigned

**INFORMATION DISCLOSURE STATEMENT (IDS)**

MS Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the divisional patent application submitted herewith. Those patents or publications which are marked with a double asterisk (\*\*) next to the Cite No. in the attached form PTO/SB/08 are not supplied because they were previously cited by or submitted to the Office in prior applications, numbers 10/191,277, filed July 10, 2002, and 09/517,318, filed March 2, 2000, which are relied upon in this application for an earlier filing date under 35 U.S.C. 120.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(b) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references. The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0216/P216-B. A duplicate copy of this paper is enclosed.

Dated: February 24, 2004

Respectfully submitted,

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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	Not Yet Assigned
				Filing Date	
				First Named Inventor	Kie Y. Ahn
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	M4065.0216/P216-B

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	A**	4,188,415	02/1980	Takahashi et al.	
	B**	4,303,715	12/1981	Chang	
	C**	3,763,680	07/1972	Tanaka et al.	
	D**	5,153,986	10/1992	Brauer et al.	
	E**	3,934,335	01/1976	Nelson	
	F**	5,502,893	04/1996	Endoh et al.	
	G**	5,587,885	12/1996	Swamy	
	H**	3,602,635	08/1971	Romankiw	
	I**	5,557,142	09/1996	Gilmore et al.	
	J**	5,949,030	09/1999	Fasano et al.	
	K**	3,934,334	01/1976	Hanni	
	L**	4,582,564	04/1986	Shanefield et al.	
	M**	5,689,091	11/1997	Hamzehdoost et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
	N**	JP 5-144221	06/1993	Sogo		
	O**	JP 3-171760	07/1991	Koizumi		

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See attached Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	Not Yet Assigned
				Filing Date	July 3, 2002
				First Named Inventor	Kie Y. Ahn
				Group Art Unit	2814
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	M4065.0216/P216-A

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	P**	Carsten Christensen et al, "WAFER THROUGH-HOLE INTERCONNECTIONS WITH HIGH VERTICAL WIRING DENSITIES," IEEE Transactions on Components ..., Part A, Vol. 19, No. 4, December 1996; pages 516-522.*	
	Q**	Michael Gribbons et al., "FINITE-DIFFERENCE TIME-DOMAIN ANALYSIS OF PULSE PROPAGATION IN MULTICHIP MODULE INTERCONNECTS," IEEE Transactions of Components .... Vol. 16, No. 5, 1993; pages 490-497.*	
	R**	R. Downing et al., "DECOUPLING CAPACITOR EFFECTS ON SWITCHING NOISE," IEEE Transactions of Components ..., Vol. 16, No. 5, 1993 pages 484-489.*	
	S**	T. Mimura et al., "SYSTEM MODULE: A NEW CHIP-ON-CHIP MODULE TECHNOLOGY," Semiconductor Research Center, Matsushita Electrical Industrial Co., Ltd., pages 21.5.1-21.5.4.*	
	T**	R. J. Jensen, "DESIGNING FOR RELIABILITY IN HARSH ENVIRONMENTS," MCM technology, Honeywell Solid State Electronics Center 1997.*	
	U**	Evan E. Davidson et al, "LONG LOSSY LINES (L <sup>3</sup> ) AND THEIR IMPACT UPON LARGE CHIP PERFORMANCE," IEEE Transactions ..., Part B, Vol. 20, No. 4, November 1997, pages 361-375.*	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.